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MICROPROCESSOR KP580VM80A PRINCIPLE OF OPERATION

Abstract: Nowadays, there is probably no area where the computer has not reached. Hush what is the basis of these computers. Of course, if we include the KP580VM80A microprocessor among these devices, it will not be a mistake. The KR580VM80A chip is a functionally complete single-chip microprocessor with persistent instruction system used as a central processor in data processing and control devices.

Keywords: KR580VM80A, 6 micro n-MDS, frequency, ALU, Buffers and registers.

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МИКРОПРОЦЕССОР КП580ВМ80А ПРИНЦИП РАБОТЫ

Абстрактный. В наши дни, наверное, нет такой области, куда бы не проник компьютер. Тише, что лежит в основе этих компьютеров. Конечно, если к этим устройствам отнести и микропроцессор КП580ВМ80А, это не будет ошибкой. Микросхема КР580ВМ80А представляет собой функционально законченный однокристальный микропроцессор с постоянной системой команд, используемый в качестве центрального процессора в устройствах обработки данных и управления.

Ключевые слова: КР580ВМ80А, 6 микрон-МДС, частота, АЛУ, Буферы и регистры.

According to the specification, it was recommended to use an external chip to generate clock signals KR580GF24, but in fact the processor is not important for the shape and state of the clock pulses [1,2]. Most local home computers do not use the KR580GF24 because its division factor of 9 makes it unsuitable for synchronous graphics machines. The use of KR580GF24 in one of the earliest home PCs, "IRISHE", did not allow the processor and video controller to work in sync and caused the computer to slow down significantly, so the KR580GF24 was produced in the future[3,4]. Not used in graphics computers, always replaced by low-integrated counters or register-based circuitry (division factor equal to 8). Like the 8080A prototype, the processor required three power supplies: −5V, +12V, and +5V. It has also been reported that the KR580VM80A can operate in abnormal mode from a single +5V supply. It is supplied instead of +12V, "ground" instead of -5V and lowers the clock frequency to 1.4-1.5 MHz [5,6].

The processor is not an exact clone of the 8080A, due to the difference in technology. The local crystal is larger, which makes it possible to create a high-level water system. The commercial industrial consumer computer Vektor-06T also has a processor running at 3 MHz, which is 20% higher than the maximum allowed. The KR580VM80A (like the 8080 prototype) has 12 undocumented instructions. Codes #08, #10, #18, #20, #28, #30, #38 are analogues of the NOP operation; opcode #CB similar to JMP; Opcodes #DD, #ED, #FD are analogues of CALL; opcode #D9 is similar to RET [7,8]. On the Radio 86RK computer, the interrupt enable output was used as a one-bit output port for sound production.

The presence of a stack operation flag in the "processor status word" issued by the SYNC signal makes it possible to allocate a separate memory bank for the stack, but this is rarely used. In the amateur computer "UT-88" this feature is used to organize the electronic disk [9,10].

Programmers have found unconventional uses of the stack in memory block copy and fill/clear procedures where maximum performance is required. This made it possible to speed up screen scrolling, cleaning and filling by ~25%, which is important for graphics machines. For example, the graphics screen of the Corvette PC8010/PC8020 computer has a size of 48KB - cleaning and changing such a size takes a lot of CPU time[11,12].

The eight-bit arithmetic-logic unit of the microprocessor provides arithmetic and logical operations on double data expressed in two's complement codes and such processing of binary-decimal packed bits. The first register block contains 16-bit registers, address pointers (IP), 16-bit registers, stack pointers (SP), 16-bit registers, time save (WZ), 16-bit bit, increment and decrement circuits, and six. 8-bit bits. General Purpose Registers (V S D E N L) Three 16-bit registers (VS DE HL) can be used. The microprocessor executes commands in machine cycles. The number of cycles required to execute the command depends on its type and can be from one to five. Machine cycles are executed in machine cycles. The number of cycles in the cycle is determined by the command. performed and can be up to five from the track. The duration of the level cycle. the cycle clock frequency is 500 ns at a frequency of 20 MHz. In the first cycle of the machine operation, the microprocessor generates a

synchronization signal, which can be combined with it. used to organize other signals and different operating modes[13,14].

When executing commands, the microprocessor can go into one of three states: “wait,” “capture,” and “stop:,” the duration of which is determined by external control signals.

A high level signal at the RDY input ensures that program commands are automatically executed by the microprocessor at the clock frequency. If the RDY pin is set to a low level signal, the microprocessor goes into the “Standby” mode and generates a high level output signal W1 [15].

The RDY signal can be used to coordinate the operation of a microprocessor with the operation of slow-moving devices if their circulation cycle duration is more than one clock period, as well as to organize step-by-step (in cycles) execution of a command or instruction-by-instruction execution of a program.

When a high-level signal is applied to the HLD input, the microprocessor goes into the “capture” state and confirms the transition to this state by generating a high-level signal at the HLDA output [16,17].

The address and data channel buffer circuits of the microprocessor are switched to a high-resistance state, and the output control signals are switched to a low-level state (except for TR and HLDA signals). The microprocessor enters the “Capture” state in the GB cycle if a read cycle is performed and there is a high-level signal at the RDY input, and in the cycle following the TC cycle if a write cycle is performed. The HLD and HLDA signals allow you to organize a direct memory access mode for any external device that generates the HLD signal [18].

When the HLT instruction is executed, the microprocessor enters the "stop" state and places the address and data channel buffer circuits into a high-resistance state. The microprocessor exits the “stop” state when there is a high-level signal at one of its inputs:

at the SR input - the microprocessor starts working from cycle T\ cycle Ml,

at the HLD input - the microprocessor goes into the “capture” state, and after the HLD signal goes low, it returns to the “stop” state,

at the INT input - the microprocessor starts executing the interrupt cycle when stopping from the GI clock if the HLT command was preceded by the E1 “interrupt enable” command, otherwise it remains in the “stop” state [19].

REFERENCES

1. Mustofoqulov, J. A., & Bobonov, D. T. L. (2021). “MAPLE” DA SO’NUVCHI ELEKTROMAGNIT TEBRANISHLARNING MATEMATIK TAHLILI. *Academic research in educational sciences*, *2*(10), 374-379.

2. Mustofoqulov, J. A., Hamzaev, A. I., & Suyarova, M. X. (2021). RLC ZANJIRINING MATEMATIK MODELI VA UNI “MULTISIM” DA HISOBLASH. *Academic research in educational sciences*, *2*(11), 1615-1621.

3. Иняминов, Ю. А., Хамзаев, А. И. У., & Абдиев, Х. Э. У. (2021). Передающее устройство асинхронно-циклической системы. *Scientific progress*, *2*(6), 204-207.

4. Каршибоев, Ш. А., Муртазин, Э. Р., & Файзуллаев, М. (2023). ИСПОЛЬЗОВАНИЕ СОЛНЕЧНОЙ ЭНЕРГИИ. *Экономика и социум*, (4-1 (107)), 678-681.

5. Мулданов, Ф. Р., Умаров, Б. К. У., & Бобонов, Д. Т. (2022). РАЗРАБОТКА КРИТЕРИЙ, АЛГОРИТМА И ЕГО ПРОГРАММНОГО ОБЕСПЕЧЕНИЯ ДЛЯ СИСТЕМЫ ИДЕНТИФИКАЦИИ ЛИЦА ЧЕЛОВЕКА. *Universum: технические науки*, (11-3 (104)), 13-16.

6. Мулданов, Ф. Р., & Иняминов, Й. О. (2023). МАТЕМАТИЧЕСКОЕ, АЛГОРИТМИЧЕСКОЕ И ПРОГРАММНОЕ ОБЕСПЕЧЕНИЕ СОЗДАНИЯ СИСТЕМЫ РОБОТА-АНАЛИЗАТОРА В ВИДЕОТЕХНОЛОГИЯХ. *Экономика и социум*, (3-2 (106)), 793-798.

7. Ирисбоев, Ф. Б., Эшонкулов, А. А. У., & Исломов, М. Х. У. (2022). ПОКАЗАТЕЛИ МНОГОКАСКАДНЫХ УСИЛИТЕЛЕЙ. *Universum: технические науки*, (11-3 (104)), 5-8.

8. Zhabbor, M., Matluba, S., & Farrukh, Y. (2022). STAGES OF DESIGNING A TWO-CASCADE AMPLIFIER CIRCUIT IN THE "MULTISIM" PROGRAMM. *Universum: технические науки*, (11-8 (104)), 43-47.

9. Каршибоев, Ш., & Муртазин, Э. Р. (2022). ТИПЫ РАДИО АНТЕНН. *Universum: технические науки*, (11-3 (104)), 9-12.

10. Омонов С.Р., & Ирисбоев Ф.М. (2023). АВТОМАТИЗИРОВАННЫЕ СИСТЕМЫ ДЛЯ ИСПЫТАНИЙ НА ЭМС НА ОСНОВЕ ПРОГРАММНОЙ ПЛАТФОРМЫ R&S ELEKTRA. Экономика и социум, (5-1 (108)), 670-677.

11. Саттаров Сергей Абудиевич, & Омонов Сардор Рахмонкул Угли (2022). ИЗМЕРЕНИЯ ШУМОПОДОБНЫХ СИГНАЛОВ С ПОМОЩЬЮ АНАЛИЗАТОРА СПЕКТРА FPC1500. Universum: технические науки, (11-3 (104)), 17-20.

12. Якименко, И. В., Каршибоев, Ш. А., & Муртазин, Э. Р. (2023). Джизакский политехнический институт СПЕЦИАЛИЗИРОВАННОЕ МАШИННОЕ ОБУЧЕНИЕ ДЛЯ РАДИОЧАСТОТ. Экономика и социум, 1196.

13. Абдиев, Х., Умаров, Б., & Тоштемиров, Д. (2021). Структура и принципы солнечных коллекторов. In *НАУКА И СОВРЕМЕННОЕ ОБЩЕСТВО: АКТУАЛЬНЫЕ ВОПРОСЫ, ДОСТИЖЕНИЯ И ИННОВАЦИИ* (pp. 9-13).

14. Раббимов, Э. А., & Иняминов, Ю. О. (2022). ВЛИЯНИЕ ОКИСНОЙ ПЛЕНКИ НА КОЭФФИЦИЕНТЫ РАСПЫЛЕНИЯ КРЕМНИЯ. *Universum: технические науки*, (11-6 (104)), 25-27.

15. Mustafaqulov, A. A., Sattarov, S. A., & Adilov, N. H. (2002). Structure and properties of crystals of the quartz which has been growth up on neutron irradiated seeds. In *Abstracts of 2. Eurasian Conference on Nuclear Science and its Application*.

16. Yuldashev, F. (2023). HARORATI MOBIL ELEKTRON QURILMALAR ASOSIDA NAZORAT QILINADIGAN QUYOSh QOZONI. *Interpretation and researches*, *1*(1).

17. Zhabbor, M., Matluba, S., & Farrukh, Y. (2022). STAGES OF DESIGNING A TWO-CASCADE AMPLIFIER CIRCUIT IN THE “MULTISIM” PROGRAMM. Universum: технические науки, (11-8 (104)), 43-47.